

REMARKS

Applicant requests the Examiner to enter the above amendments to the claims. Claims 1-33 are being canceled. No new matter is being added. Reconsideration is respectfully requested.

In the first section, the Examiner requested that claims 1-33 be canceled per the restriction requirement. Accordingly, Applicant is canceling claims 1-33.

In the second section, the Examiner objected to claims 39 and 41 for depending on non-elected claims 5 and 7, now canceled. Applicant is amending claims 39 and 41 to correct the claim dependencies.

In the third section, the Examiner rejected claims 34-43 under 35 USC § 112 as indefinite and requested Applicant to point out examples of the circuitry and signals in the drawings. First, Applicant is amending the claims to address the Examiner's concerns regarding the association between the signal circuitry and the reference circuitry. Second, Applicant brings the Examiner's attention to Fig. 13B as an example drawing of the signals and references. The transmission lines labeled "5 bit address & control" going from the memory controller 1305 to the DRAM 1310 illustrate signal transmission lines for transmitting "a first set of signals." The two transmission lines labeled "9 bit data" going from the memory controller 1305 to the DRAM 1310 illustrate signal transmission lines for transmitting "a second set of signals." The transmission lines labeled "SSVTR0" and "/SSVTR0" between the transmission lines labeled "5 bit address & control" illustrate reference transmission lines for transmitting "a pair of complementary oscillating voltage references." The transmission lines labeled "SSVTR1" and "/SSVTR1" between the transmission lines labeled "9 bit data" signals illustrate transmission lines for transmitting "a second pair of complementary oscillating references." (As stated in the specification, "SSVTR" stands for "Source Synchronous Voltage and Timing Reference.") Similar examples of such signals and/or references can be seen in Figs. 2A, 2B, 11, 12A, 12B and 13A. Example characteristics of "a pair of complementary oscillating voltage references" are more specifically shown in Figs. 3A. Example characteristics of "a pair of complementary oscillating references" relative to an

example signal of a set of signals are shown in Fig. 3B. Other instances of the signals and/or references are also illustrated in the drawings.

Circuitry for transmitting the sets of signals is illustrated in Figs 6A and 6B. Many alternative signal drivers are also well known in the art. Further, one skilled in the art is aware of many circuit alternatives for generating oscillating signals, complementary or otherwise, onto transmission lines. However, Applicant respectfully submits that one skilled in the art is completely unaware of any technique for using a pair complementary oscillating signals as complementary oscillating “voltage references” for comparison against signals, to enable level conversion of the signals, as claimed.

In the fourth section, the Examiner rejected claims 34, 36-38 and 40-43 under 35 USC § 102 as anticipated by Koide. Koide teaches comparing a single-ended signal to a fixed voltage reference to determine whether the signal is high or low. However, Koide makes no mention of transmitting “a pair of complementary oscillating voltage references” for effecting level conversion. It will be appreciated by one skilled in the art that, since the voltage reference of the invention is oscillating, the voltage difference between a signal and its reference may be greater than Koide. In the case where a voltage reference of an embodiment of the present invention has a voltage swing equal to the voltage swing of the signal, then the voltage difference can approach a full signal swing. In the case of a fixed voltage reference as in Koide, the voltage difference between a voltage reference fixed midway between high and low will be half the voltage swing. Thus, the claimed invention offers significant advantages. Further, Koide does not show a pair of references. Still further, Koide does not show complementary references. Accordingly, Application respectfully submits that the claims are patentable over Koide before and after the amendments herein.

In the fifth section, the Examiner rejected claims 39 under 35 USC § 103 as obvious over Koide in view of Lauffer. The Examiner used Lauffer to show that the signals and reference drivers can be on the same chip. Lauffer shows an amplification inverter “34” for level conversion, this amplification inverter eliminating the need for complementary references. Applicant respectfully submits that, like Koide, Lauffer does not mention transmitting “a pair of complementary oscillating voltage references” for effecting level conversion.

In the sixth section, the Examiner indicated that claim 35 would be allowable if rewritten in independent form and if the rejection under 35 USC § 112 were overcome. Applicant is rewriting claim 35 to place it into independent form.

If the Examiner has any questions or needs any additional information, the Examiner is invited to telephone the undersigned attorney at (650) 856-6500.

If for any reason an insufficient fee has been paid, the Commissioner is hereby authorized to charge the insufficiency to Deposit Account No. 05-0150.

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